CLAIMS

What is claimed is:

1. A circuit comprising at least one input, a clock input, and an output, the circuit configured to perform a pre-charge function before an evaluate function in response to the input.

2. The circuit of claim 1, further comprising a clock generator coupled to the circuit and configured to generate pulsed clock signals in response to the input.

3. The circuit of claim 1, further comprising a pre-charge component coupled to the circuit, the pre-charge component performing the pre-charge function in response to the input and a clock signal.

4. The circuit of claim 3, wherein the clock signal is a pulsed clock signal that is generated from a clock generator.

5. The circuit of claim 3, wherein the pre-charge component pre-charges at least one internal node in response to the input.

6. The circuit of claim 1, wherein the input is an enable input, wherein the enable input indicates an evaluate cycle when the enable input is in a first logic value, and wherein the enable input indicates a pre-charge cycle when the enable input is in a second logic value.

7. The circuit of claim 1, further comprising a latch coupled to the circuit and configured to store a logic value of the input.

8. A method comprising:

receiving an input signal;

generating a pulsed clock signal in response to the input signal;

pre-charging at least one node in response to the input signal; and

evaluating at least one node in response to the input signal.

9. The method of claim 8, further comprising receiving a clock signal.

10. The method of claim 8, further comprising pre-charging at least one node after an evaluation cycle.

11. The method of claim 10, wherein the pre-charging at least one node after an evaluating cycle further includes continuing pre-charging at least one node in response to the input signal.

12. The method of claim 8, wherein the generating a pulsed clock signal further includes generating a pulsed pre-charge clock and a pulsed evaluate clock.

13. A device comprising:

a circuit;

a clock circuit coupled to the circuit; and

a pre-charge circuit coupled to the clock circuit, the pre-charging circuit pre-charging the circuit before the circuit being evaluated.

14. The device of claim 13, wherein the circuit is a dynamic circuit.

15. The device of claim 13, wherein the clock circuit generates pulsed clock signals in response to an enable signal and a global clock signal.

16. The device of claim 15, wherein the pulsed clock signals further include at least a pre-charge pulsed clock signal and an evaluate pulsed clock signal.

17. The device of claim 13, wherein the pre-charge circuit receives a pre-charge pulsed clock signal from the clock circuit and pre-charges the circuit before an evaluate cycle.

18. The device of claim 13, wherein the pre-charge circuit pre-charges the circuit after the circuit being evaluated.

19. The device of claim 18, wherein the pre-charge circuit continues to pre-charge the circuit in response to an enable input.

20. A device comprising:

a first inverter having an input and an output, the input of the first inverter being coupled to a clock signal;

a latch having an input, a control input, and an output, the input of the latch being coupled to an input and the control input of the latch being coupled to the output of the first inverter;

a clock circuit having first, second, third inputs and a first, second outputs, the first input of the clock circuit being coupled to the output of the latch, the second input of the clock circuit being coupled to the output of the first inverter, and the third input of the clock circuit being coupled to the clock signal;

a second inverter having an input and an output, the input of the second inverter being coupled to the output of the latch;

a logic AND-gate having a first input, a second input, and an output, the first input of the logic AND-gate being coupled to the output of the second inverter and the second input of the logic AND-gate being coupled to the first output of the clock circuit;

a circuit having first, second, third inputs and an output, the first input of the circuit being coupled to the output of the logic AND-gate, the second input of the circuit being coupled to a data input, and the third input of the circuit being coupled to the second output of the clock circuit.

21. The device of claim 20, wherein the clock circuit further includes

a third inverter having an input and an output, the input of the third inverter being coupled to the clock signal;

a fourth inverter having an input and an output, the input of the fourth inverter being coupled to the output of the third inverter;

a logic NOR gate having a first input, a second input, and an output, the first input of the logic NOR gate being coupled to the enable input and the second input of the logic NOR gate being coupled to the output of the fourth inverter;

a first p-type transistor having source, drain, and gate terminals, the source terminal of the first p-type transistor being coupled to a first power supply, the drain terminal of the first p-type transistor being coupled to a first node;

a first n-type transistor having source, drain, and gate terminals, the drain terminal of the first n-type transistor being coupled to the first node, the gate terminal of the first n-type transistor being coupled to the output of the logic NOR gate;

a second n-type transistor having source, drain, and gate terminals, the drain terminal of the second n-type transistor being coupled to the source terminal of the first n-type transistor, the source terminal of the second n-type transistor being coupled to a second power supply, the gate terminal of the second n-type transistor being coupled to the clock signal;

a fifth inverter having an input and an output, the input of the fifth inverter being coupled to the first node;

a second p-type transistor having source, drain, and gate terminals, the source terminal of the second p-type transistor being coupled to the first power supply, the drain terminal of the second p-type transistor being coupled to the first node, the gate of the second p-type transistor being coupled to the output of the fifth inverter;

a sixth inverter having an input and an output, the input of the sixth inverter being coupled to the output of the fifth inverter;

a seventh inverter having an input and an output, the input of the seventh inverter being coupled to the output of the sixth inverter;

an eighth inverter having an input and an output, the input of the eighth inverter being coupled to the output of the seventh inverter, the output of the eighth inverter being coupled to the gate terminal of the first p-type transistor.

22. The device of claim 21, wherein the first power supply voltage is Vcc.

23. The circuit of claim 21, wherein the second power supply voltage is ground.

24. The circuit of claim 21, wherein the clock signal is a global clock signal.

25. The circuit of claim 21, wherein the input is an enable input.